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Claim 1 (currently amended) A testing method for semiconductor integrated circuits ~~wherein~~, ~~in the~~ said testing method testing by a semiconductor testing apparatus having a comparison judgment circuit judging a semiconductor integrated circuit integrated with a plurality of DA converters and a base voltage generation circuit determining ~~the~~ gradation output voltage characteristics, by comparison of ~~the~~ gradation output voltages of the semiconductor integrated circuit and reference voltages, ~~wherein~~ comprising:

deciding ~~the~~ gradation level intervals to be the test objects ~~are decided~~ by the setting of different voltages to be applied at the base power supply input terminals of said base voltage generation circuit; ~~and~~

supplying said gradation output voltages ~~are supplied~~ at and between said voltages applied to said base power supply input terminals from said semiconductor testing apparatus; and

based on a ~~by assigning~~ correspondence between ~~the~~ input gradation data signals of the gradation levels ~~of that~~ for a gradation level interval, and the gradation output voltages, testing the gradation output voltage ~~testing~~ through said semiconductor testing apparatus ~~is made to be~~ by making a digital judgment.

Claim 2 (currently amended) A testing method for semiconductor integrated circuits according to claim 1, wherein,

according to the gradation output voltages provided at and between the voltages applied to said base power supply input terminals from said semiconductor testing apparatus, said base voltage generation circuit increases or decreases the neighboring gradation output potential differences of every analog voltage output of said semiconductor integrated circuit.

Claim 3 (previously presented) A testing method for semiconductor integrated circuits according to claim 1, wherein,

by assigning correspondence between the voltage settings provided from said semiconductor testing apparatus and the input data, said DA converters and the base voltage generation circuit selectively test the output levels of the analog voltage outputs.

Claim 4 (currently amended) A testing method for semiconductor integrated circuits according to claim 1, wherein,

~~proving of the~~ reliability of the test accuracy ~~is made possible~~ is acomplished by treating the mutual relationship between the computation of the input data corresponding to every output voltage level and of ~~the~~ expectation values of the output voltages in ~~the~~ a semiconductor integrated circuit specification and ~~the~~ setting of the output voltage expectation value levels, and ~~the~~ voltage judgment value levels of said comparison judgment circuit carrying out the judgment of the output voltages, and

~~the~~ change of the setting of the test numbers with time, altogether as address or parameter management.

CLAIMS 5 THROUGH 14 ARE CANCELLED